INTEL Docket No.: P18061

Substitute for form 1449A/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Numb r**	Not yet assigned
				Filing Date	Herewith
				First Named Inventor	KESHAVARZI, Ali
(use as many sheets as necessary)				Group Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	1	of	1	INTEL Docket Number	P18061

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
TTN	A	Ohsawa, Takashi et al., "Memory Design Using a One-Transistor Gain Cell on SOI, IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, ISSN: 0018-9200, pp. 1510-1522.	
TTN	B	Thompson, Scott, et al., "MOS Scaling: Transistor Challenges for the 21st Century", Intel Technology Journal Q3'98. 19pgs.	
TTN	C	Ohsawa, Takashi et al., "ISSCC 2002/Session 9/Dram and Ferroelectric Memories / 9.1", Memory LSI Research and Development Center, Yokohama, Japan. 3pgs.	
TTN	D	Brand, A., "Intel's 0.25 Micron, 2.0Volts Logic Process Technology", Intel Technology Journal Q3'98. 9pgs.	

Examiner Signature		Date Considered	8/16/2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.